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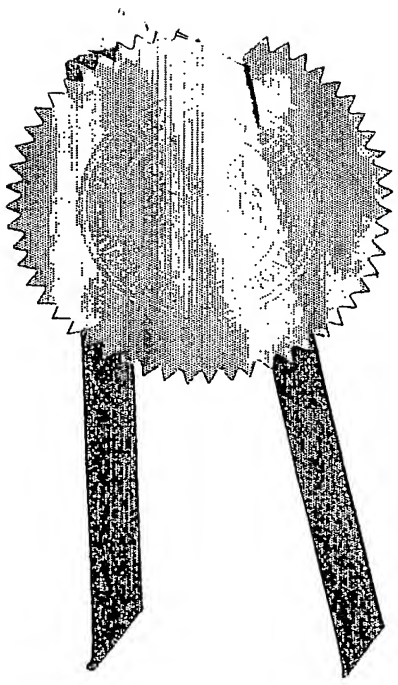
Date of Filing	:	25 SEPTEMBER 2002
Application Number	:	200205833-7
Applicant(s) / Proprietor(s) of Patent	:	WACKER SILTRONIC SINGAPORE PTE LTD
Title of Invention	:	TWO LAYER LTO BACKSIDE SEAL FOR A WAFER



SERENE CHAN (Ms)
Assistant Registrar
for REGISTRAR OF PATENTS

PRIORITY DOCUMENT
SUBMITTED OR TRANSMITTED IN COMPLIANCE WITH RULE 17.1(a) OR (b)

ACTION

PATENTS FORM 1
Patents Act
(Cap. 221)
Patents Rules
Rule 19

INTELLECTUAL PROPERTY OFFICE OF SINGAPORE

REQUEST FOR THE GRANT OF A PATENT UNDER SECTION 25

101101

* denotes mandatory fields

1. YOUR REFERENCE* MJ/JOL/aa/PAT/8110698/SG

2. TITLE OF INVENTION* TWO LAYER LTO BACKSIDE SEAL FOR A WAFER

3. DETAILS OF APPLICANT(S)* (see note 3) Number of applicant(s) 01

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State Country SG

[X] For corporate applicant [ ] For individual applicant

State of incorporation State of residency

Country of incorporation SINGAPORE Country of residency

[ ] For others (please specify in the box provided below)

(B) Name

Address

State Country

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☐ For corporate applicant

State of incorporation

Country of incorporation

☐ For individual applicant

State of residency

Country of residency

☐ For others (please specify in the box provided below)

(C) Name

Address

State

Country

☐ For corporate applicant

State of incorporation

Country of incorporation

☐ For individual applicant

State of residency

Country of residency

☐ For others (please specify in the box provided below)

☐ Further applicants are to be indicated on continuation sheet 1

4. DECLARATION OF PRIORITY (see note 5)

A. Country/country designated

File number

Filing Date DD MM YYYY

B. Country/country designated

File number

Filing Date DD MM YYYY

☐ Further details are to be indicated on continuation sheet 6

5. INVENTOR(S)* (see note 6)

A. The applicant(s) is/are the sole/joint inventor(s) Yes ☐ No ☒

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B. A statement on Patents Form 8 ~~is/will be~~ furnished Yes [X] No [ ]

6. CLAIMING AN EARLIER FILING DATE UNDER (see note 7)

[ ] section 20(3) [ ] section 26(6) [ ] section 47(4)

Patent application number

DD MM YYYY

Filing Date

Please mark with a cross in the relevant checkbox provided below
(Note: Only one checkbox may be crossed.)

[ ] Proceedings under rule 27(1)(a)

DD MM YYYY

Date on which the earlier application was amended

[ ] Proceedings under rule 27(1)(b)

7. SECTION 14(4)(C) REQUIREMENTS (see note 8)

Invention has been displayed at an international exhibition. Yes [ ] No [X]

8. SECTION 114 REQUIREMENTS (see note 9)

The invention relates to and/or used a micro-organism deposited for the purposes of disclosure in accordance with section 114 with a depository authority under the Budapest Treaty.

Yes [ ] No [X]

9. CHECKLIST*

(A) The application consists of the following number of sheets

i.	Request	5	Sheets
ii.	Description	11	Sheets
iii.	Claim(s)	15	Sheets
iv.	Drawing(s)	1	Sheets
v.	Abstract (Note: The figure of the drawing, if any, should accompany the abstract)	1	Sheets
Total number of sheets		33	Sheets

(B) The application as filed is accompanied by:

[ ] Priority document(s) [ ] Translation of priority document(s)

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[X] Statement of inventorship & right to grant

[ ] International exhibition certificate

10. DETAILS OF AGENT (see notes 10, 11 and 12)

Name

Firm: DREW & NAPIER LLC

11. ADDRESS FOR SERVICE IN SINGAPORE* (see note 10)

Block/Hse No. | Level No. | Unit No./PO Box: 152

Street Name: ROBINSON ROAD

Building Name

Postal Code: 900302

12. NAME, SIGNATURE AND DECLARATION (WHERE APPROPRIATE) OF APPLICANT OR AGENT* (see note 12)
(Note: Please cross the box below where appropriate.)

[X] I, the undersigned, do hereby declare that I have been duly authorised to act as representative, for the purposes of this application, on behalf of the applicant(s) named in paragraph 3 herein.

Name and Signature
(DREW & NAPIER LLC)

DD MM YYYY: 24 09 2002

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NOTES:

1. This form when completed, should be brought or sent to the Registry of Patents together with the rest of the application. Please note that the filing fee should be furnished within the period prescribed.

2. The relevant checkboxes as indicated in bold should be marked with a cross where applicable.

3. Enter the name and address of each applicant in the spaces provided in paragraph 3.
   Where the applicant is an individual
   - Names of individuals should be indicated in full and the surname or family name should be underlined.
   -The address of each individual should also be furnished in the space provided.
   - The checkbox for "For individual applicant" should be marked with a cross.

   Where the applicant is a body corporate
   - Bodies corporate should be designated by their corporate name and country of incorporation and, where appropriate, the state of incorporation within that country should be entered where provided.
   - The address of the body corporate should also be furnished in the space provided.
   - The checkbox for "For corporate applicant" should be marked with a cross.

   Where the applicant is a partnership
   - The details of all partners must be provided. The name of each partner should be indicated in full and the surname or family name should be underlined.
   - The address of each partner should also be furnished in the space provided.
   - The checkbox for "For others" should be marked with a cross and the name and address of the partnership should be indicated in the box provided.

4. In the field for "Country", please refer to the standard list of country codes made available by the Registry of Patents and enter the country code corresponding to the country in question.

5. The declaration of priority in paragraph 4 should state the date of the previous filing, the country in which it was made, and indicate the file number, if available. Where the application relied upon in an International Application or a regional patent application e.g. European patent application, one of the countries designated in that application [being one falling under section 17 of the Patents Act] should be identified and the country should be entered in the space provided.

6. Where the applicant or applicants is/are the sole inventor or the joint inventors, paragraph 5 should be completed by marking with a cross the 'YES' checkbox in the declaration (A) and the 'NO' checkbox in the alternative statement (B). Where this is not the case, the 'NO' checkbox in declaration (A) should be marked with a cross and a statement will be required to be filed on Patents Form 8.

7. When an application is made by virtue of section 20(3), 26(6) or 47(4), the appropriate section should be identified in paragraph 6 and the number of the earlier application or any patent granted thereon identified. Applicants proceeding under section 26(6) should identify which provision in rule 27 they are proceeding under. If the applicants are proceeding under rule 27(1)(a), they should also indicate the date on which the earlier application was amended.

8. Where the applicant wishes an earlier disclosure of the invention by him at an International Exhibition to be disregarded in accordance with section 14(4)(c), then the 'YES' checkbox at paragraph 7 should be marked with a cross. Otherwise, the 'NO' checkbox should be marked with a cross.

9. Where in disclosing the invention the application refers to one or more micro-organisms deposited with a depository authority under the Budapest Treaty, then the 'YES' checkbox at paragraph 8 should be marked with a cross. Otherwise, the 'NO' checkbox should be marked with a cross. Attention is also drawn to the Fourth Schedule of the Patents Rules.

10. Where an agent is appointed, the fields for "DETAILS OF AGENT" and "ADDRESS FOR SERVICE IN SINGAPORE" should be completed and they should be the same as those found in the corresponding Patents Form 41. In the event where no agent is appointed, the field for "ADDRESS FOR SERVICE IN SINGAPORE" should be completed, leaving the field for "DETAILS OF AGENT" blank.

11. In the event where an individual is appointed as an agent, the sub-field "Name" under "DETAILS OF AGENT" must be completed by entering the full name of the individual. The sub-field "Firm" may be left blank. In the event where a partnership/body corporate is appointed as an agent, the sub-field "Firm" under "DETAILS OF AGENT" must be completed by entering the name of the partnership/body corporate. The sub-field "Name" may be left blank.

12. Attention is drawn to sections 104 and 105 of the Patents Act, rules 90 and 105 of the Patents Rules, and the Patents (Patent Agents) Rules 2001.

13. Applicants resident in Singapore are reminded that if the Registry of Patents considers that an application contains information the publication of which might be prejudicial to the defence of Singapore or the safety of the public, it may prohibit or restrict its publication or communication. Any person resident in Singapore and wishing to apply for patent protection in other countries must first obtain permission from the Singapore Registry of Patents unless they have already applied for a patent for the same invention in Singapore. In the latter case, no application should be made overseas until at least 2 months after the application has been filed in Singapore, and unless no directions had been issued under section 33 by the Registrar or such directions have been revoked. Attention is drawn to sections 33 and 34 of the Patents Act.

14. If the space provided in the patents form is not enough, the additional information should be entered in the relevant continuation sheet. Please note that the continuation sheets need not be filed with the Registry of Patents if they are not used.

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TWO LAYER LTO BACKSIDE SEAL FOR A WAFER

FIELD OF INVENTION

The invention relates to a process for Low Temperature Oxide (LTO) deposition of a backside seal for wafers using Low Pressure Plasma Enhanced Chemical Vapour Deposition (LPPECVD) and in particular to a two layer LTO backside seal.

BACKGROUND

Autodoping is a problem that occurs in silicon wafers that are used for epitaxial deposition. During the heat cycle of the epitaxial process, the highly doped (p+) silicon substrates diffuse out dopant atoms through the backside of the substrate leading to an unintentional overdoping effect on the wafer frontside. This is most noticeable at the edge of the wafer. This leads to an inhomogeniety in the epitaxial dopant profile beyond the tolerance of most device manufacturers.

A backside layer on the wafer reduces the autodoping effect.

Various technologies are used for the deposition of a SiO_2 layer. These can roughly be divided into atmospheric and low-pressure applications and further into processes that utilize the ignition of plasma (plasma enhanced: PE) in chemical vapour deposition (CVD), which makes used of pyrolytic surface-catalysis of silicon and oxygen bearing carrier gases.

Haze or epi-haze is non-localised light scattering resulting from uneven surface topography (micro-roughness) or from dense concentrations of surface or near surface imperfections. Semiconductor wafers should have low or no epi-haze.

Film stress is the compressive or tensile forces that affect the film on a wafer. A wafer layer with high film stress is more vulnerable to warpage than a wafer layer with low film stress.

One existing system provides a single LTO layer on the backside of a wafer. However the layer produced is typically thicker than 500 nm and does not solve the problems of haze on the front face of the wafer and warpage of the wafer.

SUMMARY OF INVENTION

In broad terms in one aspect the invention comprises a two layer LTO backside seal for a wafer having a first major side and a second major side comprising: a low stress LTO layer having a first major side and a second major side, the first major side of the low stress LTO layer adjacent to one major side of the wafer; and a high stress LTO layer having a first major side and second major side, the first major side of the high stress LTO layer adjacent the second major side of the low stress LTO layer.

In broad terms in a further aspect the invention comprises a method of forming a two layer LTO backside seal for a wafer having two major sides including the steps of forming a low stress LTO layer having a first major side and second major side with the first major side on one major side of the wafer and forming a high stress LTO layer with a first major side and second major side on the second major side of the low stress LTO layer.

In broad terms in a further aspect the invention comprises a pp+ silicon epitaxial wafer including, a p+ substrate a first major side and a second major side, a low stress LTO layer having a first major side and a second major side, the first major side of the low stress LTO layer adjacent the first major side of the p+ substrate, and a high stress LTO silicon oxide layer having a first major side and a second major side, the first major side of the high stress LTO silicon oxide layer adjacent the second major side of the low stress LTO layer.

In broad terms in a further aspect the invention comprises an nn+ silicon epitaxial wafer including, an n+ substrate a first major side and a second major side, a low stress LTO layer having a first major side and a second major side, the first major side of the low stress LTO layer adjacent the first major side of the n+ substrate, and a high stress LTO

silicon oxide layer having a first major side and a second major side, the first major side of the high stress LTO silicon oxide layer adjacent the second major side of the low stress LTO layer.

BRIEF DESCRIPTION OF DRAWINGS

Preferred form wafers of the invention will be further described with reference to the accompanying drawings by way of example only and without intending to be limiting, wherein;

Figure 1 shows a silicon wafer with a two layer LTO backside seal; and

Figure 2 shows a silicon wafer with a LTO backside seal after deposition of an epitaxial layer on the wafer frontside.

DETAILED DESCRIPTION

Figure 1 shows a silicon wafer with two LTO layers forming a backside seal. Substrate 1 is the doped (either p-type or n-type) silicon. Layer 2 is a low stress LTO layer formed using high frequency RF at high power with high silane (SiH_4) flow. Layer 3 is deposited on layer 2 using both high and low frequency RF at high power to provide a high density high stress LTO layer with low etch rate during subsequent cleaning processes.

The low stress LTO layer 2 controls the geometry of the wafer to minimise wafer warpage. The low stress LTO layer further acts to improve epi-haze during epitaxy.

The high stress LTO layer has high density and therefore a low etch rate. This allows the backside seal to maintain the low stress LTO layer during subsequent cleaning processes as only a small amount of the high stress LTO layer is available for etching. The low stress LTO layer also has high deposition rate, which means a high throughput. A high stress LTO layer with low etch rate provides a reduction in production costs.

LTO plasma processes commonly use N_2 for dilution, N_2O as an oxygen carrying gas, and SiH_4 as a silicon carrying gas. In the plasma phase these compounds are dissociated into their respective ionic components and the more mobile electrons are accelerated by high frequency RF at high power coupled to the reaction chamber to strike the plasma. There is a small negative voltage between the positive ions in the plasma and the wafer that rests on a grounded heater block. This potential difference will accelerate the ions towards the wafer surface where the ions form a layer of silicon dioxide (SiO_2).

High and low frequency RF power is commonly used in LTO reactors to enhance the LPCVD process. High frequency RF power is used to strike the plasma by accelerating the electrons whereas low frequency RF power is used to enhance the densification of the layer to be formed as it keeps heavier ions mobile for an extended time.

Using the method of the invention a wafer is formed with a double layer LTO backside seal in which the inner layer has low stress and the outer layer has high stress. The stress of the inner layer is typically < 100 Mpa and the stress of the outer layer is typically < 300 Mpa. The inner layer controls the epi-haze of the wafer and the geometry of the wafer. The outer layer controls the thickness reduction of the backside layer during wet bench cleaning.

Table 1 shows a set of steps for producing a wafer with a double layer LTO backside seal.

	Step 1	Step 2	Step 3	Step 4	Step 5	Step 6	Step 7	Step 8	Step 9	Step 10
Pressure (Pa)	0	200 - 467	200 - 467	200 - 467	200 - 467	200 - 467	200 - 467	200 - 467	200 - 467	0
Time (sec)	1 - 50	1 - 50	1 - 50	1 - 50	Varies depending on specified thickness of layer	Varies depending on specified thickness of layer	1 -50	1 -50	1 -50	1- 50
Dump (sec)	0	0	0	0 - 20	0	0	0	0	0	0
Temperature (°C)	250 – 600, typically 300 - 450	250 – 600, typically 300 - 450	250 – 600, typically 300 - 450	250 – 600, typically 300 - 450	250 – 600, typically 300 - 450	250 – 600, typically 300 - 450	250 – 600, typically 300 - 450	250 – 600, typically 300 - 450	250 – 600, typically 300 - 450	250 – 600, typically 300 - 450
HF RF power (w)	0	0	0	0	200 - 1600 typically 300 - 1200	200 - 1600 typically 300 - 1200	200 - 1600 typically 300 - 1200	0	0	0
LF RF power (w)	0	0	0	0	0 - 800 typically 100 - 600	0 - 800 typically 100 - 600	0 - 800 typically 100 - 600	0	0	0
N_2 (sccm)	0	800 - 7000 typically 1000-4000	800 - 7000 typically 1000-4000	800 - 7000 typically 1000-4000	800 - 7000 typically 1000-4000	800 - 7000 typically 1000-4000	800 - 7000 typically 1000-4000	800 - 7000 typically 1000-4000	800 - 7000 typically 1000-4000	0
N_2O (sccm)	0	0	2000 – 18000 typically 3000 - 15000	2000 – 18000 typically 3000 - 15000	2000 – 18000 typically 3000 - 15000	2000 – 18000 typically 3000 - 15000	2000 – 18000 typically 3000 - 15000	2000 – 18000 typically 3000 - 15000	0	0
SiH_4 (sccm)	0	0	0	50 – 1000 typically 100 - 600	50 – 1000 typically 100 - 600	50 – 1000 typically 100 - 600	0	0	0	0

Table 1

Step 5 of Table 1 shows preferred ranges for pressure, time, temperature, high RF frequency power, low RF frequency power, N_2, N_2O, and SiH_4 so that a low stress LTO layer is formed. To form the low stress LTO layer requires high silane flow, low frequency RF at low power, high frequency RF at high power, and low pressure. Ideally the flow rates, power, pressure etc are chosen from the ranges provided in Table 1. This combination of parameters generates a high deposition rate (typically 5000 – 12000 Å/min) and results in a low stress SiO_2 layer. This layer typically is an imperfect SiO_2 network. This layer will keep the wafer in almost stress free status and improve the epi-haze level. Using this layer the epi-haze level of the wafer will be reduced to typically 0.1 – 1 ppm. The high frequency RF at high power generates a high deposition rate and low film stress. The low pressure in this step assists in creating the high deposition rate, as does the high silane rate. Depositing a low stress layer onto the wafer results in low bow and warp on the wafer after epitaxy deposition. This is difficult to achieve with existing single-layer LTO backside seals, especially those thicker than 500 nm.

Step 6 of Table 1 shows preferred ranges for pressure, time, temperature, high RF frequency power, low RF frequency power, N_2, N_2O, and SiH_4 so that a high stress LTO layer is formed. To form the high stress LTO layer requires low frequency RF at high power, higher pressure, and low silane flow. Ideally the flow rates, power, pressure etc are chosen from the parameters provided in Table 1. The combination of parameters in step 6 will result in low deposition rate and generate a high density LTO layer. To form the high stress LTO layer the low frequency RF power is chosen to be higher than in step 5, the silane flow is chosen to be lower than in step 5 and the pressure is chosen to the higher than in step 5. The high stress LTO layer has a lower etch rate in wet bench processes (which involve HF solutions) preferably equal to about one quarter of the etch rate of the low stress layer formed in step 5. The low frequency RF at high power serves to accelerate ion movement to bombard the deposited layer forming a high stress, high density layer that has a low etch rate. The high deposition pressure assists in creating a low deposition rate and a high density film with high film stress. The low silane flow also assists in creating a low deposition rate, and a high density film with high stress.

In the process used to form the LTO backside seal the high frequency RF is typically 13.56 MHz as this is the industry standard but may be any suitable frequency. The low frequency RF is typically between 100 kHz and 600 kHz. More typically the low RF frequency is 200 kHz as this is the industry standard but may be any suitable frequency.

The combination of the high stress and low stress LTO layers provides significantly greater suppression of visual edge epi-haze over existing single-layer LTO backside seal devices. The double layer backside seal has a high deposition rate. This rate is ideally about three times higher than for an existing single layer LTO backside seal showing time effectiveness in deposition of the two-layer backside seal.

The deposition of the low stress and high stress LTO layers is ideally a continual plasma process. This assists in forming a network between the two LTO backside seal layers. The advantages of forming a network between the high stress and low stress layers include low wafer bow and warp even after epitaxy deposition as will be further described below. This advantage is not affected by the thickness of the LTO backside seal.

The low stress LTO layer deposited with the process recipe of Table 1 has a much higher etch rate in wet bench processes and epitaxy than the high stress LTO outer film. The high stress LTO backside seal layer has a low etch rate in wet bench processes. The outer high stress LTO layer has no stress release during epitaxial high temperature annealing and provides no contribution to the final geometry of the wafer during epitaxy. The only contribution to the final geometry of the wafer during epitaxy is from the frontside epitaxy layer and has some relation to epitaxy thickness.

Referring back to Figure 1, this Figure shows the silicon wafer 1 with inner low stress LTO layer 2 and outer high stress LTO layer 3. The high stress LTO layer 3 has a lower etch rate than the low stress LTO layer 2 because of the different densities of the layers. After the cleaning process the different etch rates will cause the high stress LTO layer 3 to extend over the low stress LTO layer 2 before epitaxy annealing. This may be

overcome by removal of some of the thickness of the high stress LTO layer during the cleaning process.

After the two layer LTO backside seal is formed on the wafer the wafer is subjected to LTO edge removal to remove any LTO film on the edge area of the wafer and any trace LTO film on the wafer front side. The edge exclusion is typically 0.006 to 5 mm. This process does not reduce the thickness of the high stress outer LTO layer.

Following the edge removal process the wafer is subjected to edge polishing and edge polish cleaning. The edge polishing process does not remove any of the LTO film form the backside of the wafer. Edge polish cleaning uses a solution of HF/O_3 with HF concentration of typically 0.02 to 0.5%. The edge polish cleaning process typically removes 5 – 30 nm from the thickness of the LTO backside seal.

After polishing and polish cleaning a post-polish clean is performed. The post-polish clean further removes some of the LTO layer. The concentration of HF in the post-polish clean is typically 0.1 – 1% resulting in removing typically 10 – 50 nm of the thickness of the LTO backside seal.

Before epitaxy at least one wet bench cleaning is necessary. The wet bench clean typically includes 0.1 – 1% HF which results in LTO backside seal thickness removal of 1 – 30 nm.

One method to control the sharp edge shape of the outer high stress LTO layer 3 is as follows: during the first wet bench process the inner low stress LTO layer 2 with the higher etch rate than the high stress LTO layer is etched, which leaves part of the high stress LTO layer overhanging the low stress LTO layer. When this occurs the exposed underside of the high stress LTO layer will be etched as well as the top of the high stress LTO layer leading to the overhanging portion of the high stress LTO layer having twice the etch rate as the remainder of the high stress LTO layer. Therefore, even before epitaxy the edge shape of the outer high stress LTO layer is controlled through top thickness control.

The double layer LTO backside seal has another effect on post-epi warpage. The outer high stress layer of the LTO backside seal has no film stress release during epitaxy. It is well known that a PECVD LTO film contains a large amount of by-elements and is an imperfect network. For example SiO_x, $SiNH_x$ and SiH_x (where x= 1, 2, 3, 4) are some of the by-elements. A more porous LTO layer has more by-elements. During epitaxy high temperature annealing (typically at temperatures of 1050 to 1200 °C) by-element outgasing and film network rearranging occurs. During epitaxy the LTO layer will tend to become a high density layer, which has almost the same properties as thermal silicon oxidation, e.g. a similar post-epi etching rate. This means that after epitaxy high temperature annealing the LTO film will have almost the same properties as thermal oxidation regardless of the deposition process used. The double layer LTO backside seal has the same etch rate after epitaxy as a single layer LTO backside seal. This is shown in Figure 2 where a layer of epitaxial material 5 has been deposited on wafer 1 and the high stress and low stress LTO layers have densified to form a single LTO layer 4.

During epitaxy further reductions occur in the thickness of the backside seal. In the high stress layer typically 2 – 6% of the thickness is lost during epitaxy. For the low stress layer typically 3 – 10% of the thickness is lost. The loss of thickness in the inner low stress LTO layer relates to rearrangement of the LTO film network as described above.

However the backside seal of the invention will still have a lower etching rate in HF solution. This is because during epitaxy high temperature annealing only hydrogen elements can be outgased and nitrogen elements will be incorporated with the silicon bond. This creates a Si-O-N network in the LTO backside seal that has high density and low etch rate. During the rearrangement of the network of the LTO backside seal the density of the inner low stress layer increases followed by the density of the outer high stress layer. As both the high stress and low stress LTO layers belong to the same network and are formed from the same material there is a better connection between these layers than the connection between the inner layer and the wafer. This will

control the wafer geometry to reduce warpage and keep the beneficial low etch rate of the high stress layer.

Comparing the two layer LTO backside seal described above and existing single layer backside seals shows a benefit of the two layer LTO backside seal. Before epitaxy both of the seals provide almost the same contribution to the geometry of the wafer. After epitaxy the single layer LTO seal provides a high stress contribution that increases warpage of the wafer, but the double layer LTO seal maintains the same wafer geometry. This effect is impossible to achieve with a single layer backside seal, especially with a thick backside seal (typically > 500 nm).

As well as the double layer LTO backsides seal a polysilicon layer may be included between the wafer and the double layer LTO backside seal. Preferably the thickness of the polysilicon layer is between 0.5 and 2 microns. The polysilicon layer acts as an external gettering for impurity and metal contamination.

A typical double layer LTO backside seal formed using the method described herein preferably is between 1000 and 10000 Å thick. A wafer with a typical epi-thickness of between 1 micron and 20 microns and with a double layer LTO backside seal will typically have warp of less than 50 microns, more typically less than 30 microns, and most typically less than 25 microns as measured by an ADE capacitive tool. The wafer will typically further have bow of less than 30 microns, more typically less than 20 microns, and most typically less than 15 microns as measured with an ADE capacitive tool. The typical localised light scatterers (LLS) of a wafer with a double layer LTO backside seal, as measured with a KLA Tencor SP1 or equivalent laser scattering tool, is: LLS > 0.128 microns, less than 100 per wafer and typically less than 30 per wafer; LLS > 0.155 microns, less than 50 per wafer and typically less than 10 per wafer; LLS > 0.193 microns, less than 30 per wafer and typically less than 10 per wafer; LLS > 0.285 microns, less than 20 per wafer and typically less than 5 per wafer. The haze performance is typically less than 50 ppm, more typically less than 20 ppm, and most typically less than 15 ppm. This shows very good haze and LLS performance for

wafers with a double-layer LTO backside seal. The double layer LTO backside seal also has a typical etch rate in wet bench cleaning or less than 100 nm.

The silicon epitaxial wafer may be a pp+ wafer having a p-type epitaxy layer and a p+ substrate. Alternatively the silicon epitaxial wafer may be a nn+ wafer have an n-type epitaxy layer and an n+ substrate.

The foregoing describes the invention including a preferred form thereof. Alterations and modifications as will be obvious to those skilled in the art are intended to be incorporated within the scope hereof as defined in the accompanying claims.

CLAIMS

1. A two layer LTO backside seal for a wafer having a first major side and a second major side comprising:

a low stress LTO layer having a first major side and a second major side, the first major side of the low stress LTO layer adjacent of one major side of the wafer; and

a high stress LTO layer having a first major side and second major side, the first major side of the high stress LTO layer adjacent the second major side of the low stress LTO layer.

2. A two layer LTO backside seal for a wafer as claimed in claim 1 wherein the low stress LTO layer is formed using high frequency RF power.

3. A two layer LTO backside seal for a wafer as claimed in claim 2 wherein the power of the high frequency RF is between 200 and 1600 watts.

4. A two layer LTO backside seal for a wafer as claimed in claim 2 or claim 3 wherein power of the high frequency RF is between 300 and 1200 watts.

5. A two layer LTO backside seal for a wafer as claimed in any one of claims 2 to 4 wherein the high frequency used in forming the low stress LTO layer is about 13.56MHz.

6. A two layer LTO backside seal for a wafer as claimed in any one of claims 1 to 5 wherein the low stress layer is formed using low pressure.

7. A two layer LTO backside seal for a wafer as claimed in claim 6 wherein the pressure used to form the low stress LTO layer is between 200 and 467 Pa.

8. A two layer LTO backside seal for a wafer as claimed in any one of claims 1 to 7 wherein the low stress LTO layer is formed using high silane flow rate.

9. A two layer LTO backside seal for a wafer as claimed in claim 8 wherein the silane flow used to form the low stress LTO layer is between 50 and 1000 sccm.

10. A two layer LTO backside seal for a wafer as claimed in claim 8 or claim 9 wherein the silane flow used to form the low stress LTO layer is between 100 and 600 sccm.

11. A two layer LTO backside seal for a wafer as claimed in any one of claims 1 to 10 wherein the temperature used to form the low stress LTO layer is between 250 and 600°C.

12. A two layer LTO backside seal for a wafer as claimed in any one of claims 1 to 11 wherein the temperature used to form the low stress LTO layer is between 300 and 450°C.

13. A two layer LTO backside seal for a wafer as claimed in any one of claims 1 to 12 wherein the low stress LTO layer is formed in the presence of N_2 with flow rate between 800 and 7000 sccm.

14. A two layer LTO backside seal for a wafer as claimed in any one of claims 1 to 13 wherein the N_2 flow rate used in the formation of the low stress LTO layer is between 1000 and 4000 sccm.

15. A two layer LTO backside seal for a wafer as claimed in any one of claims 1 to 14 wherein the low stress LTO layer is formed in the presence of N_2O with flow rate between 2000 and 18000 sccm.

16. A two layer LTO backside seal for a wafer as claimed in any one of claims 1 to 15 wherein the N_2O flow rate used in the formation the low stress LTO layer is between 3000 and 15000 sccm.

17. A two layer LTO backside seal for a wafer as claimed in any one of claims 1 to 16 wherein the high stress LTO layer is formed using high frequency RF power at high power.

18. A two layer LTO backside seal for a wafer as claimed in claim 17 wherein the power of the high frequency RF is between 200 and 1600 watts.

19. A two layer LTO backside seal for a wafer as claimed in claim 17 or claim 18 wherein the power of the high frequency RF is between 300 and 1200 watts.

20. A two layer LTO backside seal for a wafer as claimed in any one of claims 17 to 19 wherein the high frequency used in forming the high stress LTO layer is 13.56 MHz.

21. A two layer LTO backside seal for a wafer as claimed in any one of claims 1 to 20 wherein the high stress LTO layer is formed using low frequency RF at high power.

22. A two layer LTO backside seal for a wafer as claimed in claim 21 wherein the high stress LTO layer is formed using low frequency RF with power between 0 and 800 watts.

23. A two layer LTO backside seal for a wafer as claimed in claim 21 or claim 22 wherein the high stress LTO layer is formed using low frequency RF with power between 100 and 600 watts.

24. A two layer LTO backside seal for a wafer as claimed in any one of claims 21 to 23 wherein the low frequency used in forming the high stress LTO layer is between 100 and 600 kHz.

25. A two layer LTO backside seal for a wafer as claimed in claim 24 wherein the low frequency used in forming the high stress LTO layer is 200 kHz.

26. A two layer LTO backside seal for a wafer as claimed in any one of claims 1 to 25 wherein the high stress layer is formed using high pressure.

27. A two layer LTO backside seal for a wafer as claimed in claim 26 wherein the high stress LTO layer is formed using higher pressure than the pressure used to form the low stress LTO layer.

28. A two layer LTO backside seal for a wafer as claimed in claim 26 or 27 wherein the pressure used to form the high stress LTO layer is between 200 and 467 Pa.

29. A two layer LTO backside seal for a wafer as claimed in any one of claims 1 to 28 wherein the high stress LTO layer is formed using low silane flow.

30. A two layer LTO backside seal for a wafer as claimed in claim 29 wherein the high stress LTO layer is formed using silane flow between 50 and 1000 sccm.

31. A two layer LTO backside seal for a wafer as claimed in claim 29 or claim 30 wherein the high stress LTO layer is formed using silane flow between 100 and 600 sccm.

32. A two layer LTO backside seal for a wafer as claimed in any one of claims 29 to 31 wherein the high stress LTO layer is formed using silane flow with a slower flow rate than that used in the step of forming the low stress LTO layer.

33. A two layer LTO backside seal for a wafer as claimed in any one of claims 1 to 32 wherein the temperature used to form the high stress LTO layer is between 250 and 600°C.

34. A two layer LTO backside seal for a wafer as claimed in any one of claims 1 to 33 wherein the temperature used to form the high stress LTO layer is between 300 and 450°C.

35. A two layer LTO backside seal for a wafer as claimed in any one of claims 1 to 34 wherein the high stress LTO layer is formed in the presence of N_2 with a flow rate between 800 and 7000 sccm.

36. A two layer LTO backside seal for a wafer as claimed in 35 wherein the N_2 flow rate used in the formation of the high stress LTO layer is between 1000 and 4000 sccm.

37. A two layer LTO backside seal for a wafer as claimed in any one of claims 1 to 36 wherein the high stress LTO layer is formed in the presence of N_2O with a flow rate between 2000 and 18000 sccm.

38. A two layer LTO backside seal for a wafer as claimed in any one of claims 1 to 37 wherein the N_2O flow rate used in the formation of the high stress LTO layer is between 3000 and 15000 sccm.

39. A two layer LTO backside seal for a wafer as claimed in any one of claims 1 to 38 wherein as the low stress and high stress LTO layers are deposited a network is formed between the low stress and high stress layers.

40. A two layer LTO backside seal for a wafer as claimed in any one of claims 1 to 39 wherein the wafer is a p-type silicon wafer.

41. A two layer LTO backside seal for a wafer as claimed in any one of claims 1 to 39 wherein the wafer is an n-type silicon wafer

42. A method of forming a two layer LTO backside seal on a wafer having two major sides including the steps of:

forming a low stress LTO layer having a first major side and second major side with the first major side on one major side of the wafer, and

forming a high stress LTO layer with a first major side and second major side with one major side of the high stress LTO layer adjacent the second major side of the low stress LTO layer.

43. A method of forming a two layer LTO backside seal on a wafer as claimed in claim 42 further including the step of forming the low stress LTO layer using high frequency RF power.

44. A method of forming a two layer LTO backside seal on a wafer as claimed in claim 43 wherein the power of the high frequency RF is between 200 and 1600 watts.

45. A method of forming a two layer LTO backside seal on a wafer as claimed in claim 43 or claim 44 wherein power of the high frequency RF is between 300 and 1200 watts.

46. A method of forming a two layer LTO backside seal on a wafer as claimed in any one of claims 43 to 45 wherein the high frequency used in forming the low stress LTO layer is about 13.56MHz.

47. A method of forming a two layer LTO backside seal on a wafer as claimed in any one of claims 42 to 46 further including the step of forming the low stress LTO layer using low pressure.

48. A method of forming a two layer LTO backside seal on a wafer as claimed in claim 47 wherein the pressure used to form the low stress LTO layer is between 200 and 467 Pa.

49. A method of forming a two layer LTO backside seal on a wafer as claimed in any one of claims 42 to 48 further including the step of forming the low stress LTO layer using high silane flow rate.

50. A method of forming a two layer LTO backside seal on a wafer as claimed in claim 49 wherein the silane flow used to form the low stress LTO layer is between 50 and 1000 sccm.

51. A method of forming a two layer LTO backside seal on a wafer as claimed in claim 49 or claim 50 wherein the silane flow used to form the low stress LTO layer is between 100 and 600 sccm.

52. A method of forming a two layer LTO backside seal on a wafer as claimed in any one of claims 42 to 51 further including the step of forming the low stress LTO layer using temperature between 250 and 600°C.

53. A method of forming a two layer LTO backside seal on a wafer as claimed in claim 52 wherein the temperature used to form the low stress LTO layer is between 300 and 450°C.

54. A method of forming a two layer LTO backside seal on a wafer as claimed in any one of claims 42 to 53 further including the step of forming the low stress LTO layer in the presence of N_2 with flow rate between 800 and 7000 sccm.

55. A method of forming a two layer LTO backside seal on a wafer as claimed in claim 54 wherein the N_2 flow rate used in the formation of the low stress LTO layer is between 1000 and 4000 sccm.

56. A method of forming a two layer LTO backside seal on a wafer as claimed in any one of claims 42 to 55 further including the step of forming the low stress LTO layer in the presence of N_2O with flow rate between 2000 and 18000 sccm.

57. A method of forming a two layer LTO backside seal on a wafer as claimed in claim 56 wherein the N_2O flow rate used in the formation the low stress LTO layer is between 3000 and 15000 sccm.

58. A method of forming a two layer LTO backside seal on a wafer as claimed in any one of claims 42 to 57 further including the step of forming the high stress LTO layer using high frequency RF power at high power.

59. A method of forming a two layer LTO backside seal on a wafer as claimed in claim 58 wherein the power of the high frequency RF is between 200 and 1600 watts.

60. A method of forming a two layer LTO backside seal on a wafer as claimed in claim 58 or claim 59 wherein the power of the high frequency RF is between 300 and 1200 watts.

61. A method of forming a two layer LTO backside seal on a wafer as claimed in any one of claims 58 to 60 wherein the high frequency used in forming the high stress LTO layer is 13.56 MHz.

62. A method of forming a two layer LTO backside seal on a wafer as claimed in any one of claims 42 to 61 further including the step of forming the high stress LTO layer using low frequency RF at high power.

63. A method of forming a two layer LTO backside seal on a wafer as claimed in claim 62 wherein the high stress LTO layer is formed using low frequency RF with power between 0 and 800 watts.

64. A method of forming a two layer LTO backside seal on a wafer as claimed in claim 62 or claim 63 wherein the high stress LTO layer is formed using low frequency RF with power between 100 and 600 watts.

65. A method of forming a two layer LTO backside seal on a wafer as claimed in any one of claims 61 to 63 wherein the low frequency used in forming the high stress LTO layer is between 100 and 600 kHz.

66. A method of forming a two layer LTO backside seal on a wafer as claimed in claim 65 wherein the low frequency used in forming the high stress LTO layer is 200 kHz.

67. A method of forming a two layer LTO backside seal on a wafer as claimed in any one of claims 42 to 66 further including the step of forming the high stress LTO layer using high pressure.

68. A method of forming a two layer LTO backside seal on a wafer as claimed in claim 67 further including the step of forming the high stress LTO layer using higher pressure than the pressure used to form the low stress LTO layer.

69. A method of forming a two layer LTO backside seal on a wafer as claimed in claim 67 or 68 wherein the pressure used to form the high stress LTO layer is between 200 and 467 Pa.

70. A method of forming a two layer LTO backside seal on a wafer as claimed in any one of claims 42 to 69 further including the step of forming the high stress LTO layer using low silane flow.

71. A method of forming a two layer LTO backside seal on a wafer as claimed in claim 70 wherein the high stress LTO layer is formed using silane flow between 50 and 1000 sccm.

72. A method of forming a two layer LTO backside seal on a wafer as claimed in claim 70 or claim 71 wherein the high stress LTO layer is formed using silane flow between 100 and 600 sccm.

73. A method of forming a two layer LTO backside seal on a wafer as claimed in any one of claims 70 to 72 wherein the high stress LTO layer is formed using silane flow with a slower flow rate than that used in the step of forming the low stress LTO layer.

74. A method of forming a two layer LTO backside seal on a wafer as claimed in any one of claims 42 to 73 further including the step of forming the high stress LTO layer using at least one temperature between 250 and 600°C.

75. A method of forming a two layer LTO backside seal on a wafer as claimed in claim 74 wherein the temperature used to form the high stress LTO layer is between 300 and 450°C.

76. A method of forming a two layer LTO backside seal on a wafer as claimed in any one of claims 42 to 75 further including the step of forming the high stress LTO layer in the presence of N_2 with a flow rate between 800 and 7000 sccm.

77. A method of forming a two layer LTO backside seal on a wafer as claimed in 76 wherein the N_2 flow rate used in the formation of the high stress LTO layer is between 1000 and 4000 sccm.

78. A method of forming a two layer LTO backside seal on a wafer as claimed in any one of claims 42 to 77 further including the step of forming the high stress LTO layer in the presence of N_2O with a flow rate between 2000 and 18000 sccm.

79. A method of forming a two layer LTO backside seal on a wafer as claimed in claim 78 wherein the N_2O flow rate used in the formation of the high stress LTO layer is between 3000 and 15000 sccm.

80. A method of forming a two layer LTO backside seal on a wafer as claimed in any one of claims 42 to 79 wherein the steps of forming the low stress and high stress LTO layers include the step of forming a network between the low stress and high stress layers.

81. A method of forming a two layer LTO backside seal on a wafer as claimed in any one of claims 42 to 80 wherein the wafer is a p-type silicon wafer.

82. A method of forming a two layer LTO backside seal on a wafer as claimed in any one of claims 42 to 80 wherein the wafer is an n-type silicon wafer.

83. A wafer formed using the method of any one of claims 42 to 82.

84. A wafer formed using the method of any one of claims 42 to 82 further including a layer of polysilicon between the wafer and the low stress layer.

85. A pp+ silicon epitaxial wafer including:

a p+ substrate a first major side and a second major side,

a low stress LTO layer having a first major side and a second major side, the first major side of the low stress LTO layer adjacent the first major side of the p+ substrate, and

a high stress LTO silicon oxide layer having a first major side and a second major side, the first major side of the high stress LTO silicon oxide layer adjacent the second major side of the low stress LTO layer.

86. A pp+ silicon epitaxial wafer as claimed in claim 85 further including an epitaxial layer on the second major side of the p+ substrate.

87. A pp+ silicon epitaxial wafer as claimed in claim 86 wherein epitaxial layer is between 1 and 50 microns thick.

88. A pp+ silicon epitaxial wafer as claimed in any one of claims 85 to 87 wherein the thickness of the low stress LTO layer and the high stress LTO layer is between 1000 A and 10000 A.

89. A pp+ silicon epitaxial wafer as claimed in any one of claims 85 to 88 further including a polysilicon layer between the substrate and the low stress LTO layer.

90. A pp+ silicon epitaxial wafer as claimed in claim 89 wherein the thickness of the polysilicon layer is between 0.5 and 2 microns.

91. A pp+ silicon epitaxial wafer as claimed in any one of claims 85 to 90 wherein the warp is less than 50 microns.

92. A pp+ silicon epitaxial wafer as claimed in claim 91 wherein the warp is less than 20 microns.

93. A pp+ silicon epitaxial wafer as claimed in any one of claims 85 to 92 wherein the bow is less than 30 microns.

94. A pp+ silicon epitaxial wafer as claimed in claim 93 wherein the bow is less than 15 microns.

95. A pp+ silicon epitaxial wafer as claimed in any one of claims 85 to 94 wherein the haze performances is less than 50 ppm.

96. A pp+ silicon epitaxial wafer as claimed in claim 95 wherein the haze performance is less than 15 ppm.

97. A pp+ silicon epitaxial wafer as claimed in any one of claims 85 to 96 wherein the LLS performance greater than 0.128 microns is less than 100 per wafer.

98. A pp+ silicon epitaxial wafer as claimed in claim 97 wherein the LLS performance greater than 0.128 microns is less than 30 per wafer.

99. A pp+ silicon epitaxial wafer as claimed in any one of claims 85 to 98 wherein the LLS performance greater than 0.155 microns is less than 50 per wafer.

100. A pp+ silicon epitaxial wafer as claimed in claim 99 wherein the LLS performance greater than 0.155 microns is less than 10 per wafer.

101. A pp+ silicon epitaxial wafer as claimed in any one of claims 85 to 100 wherein the LLS performance greater than 0.193 microns is less than 30 per wafer.

102. A pp+ silicon epitaxial wafer as claimed in claim 101 wherein the LLS performance greater than 0.193 microns is less than 10 per wafer.

103. A pp+ silicon epitaxial wafer as claimed in any one of claims 85 to 102 wherein the LLS performance greater than 0.285 microns is less than 20 per wafer.

104. A pp+ silicon epitaxial wafer as claimed in claim 103 wherein the LLS performance greater than 0.285 microns is less than 5 per wafer.

105. A pp+ silicon epitaxial wafer as claimed in any one of claims 85 to 104 wherein the etch rate in wet bench cleaning is less than 100nm.

106. An nn+ silicon epitaxial wafer including:

an n+ substrate a first major side and a second major side,

a low stress LTO layer having a first major side and a second major side, the first major side of the low stress LTO layer adjacent the first major side of the n+ substrate, and

a high stress LTO silicon oxide layer having a first major side and a second major side, the first major side of the high stress LTO silicon oxide layer adjacent the second major side of the low stress LTO layer.

107. An nn+ silicon epitaxial wafer as claimed in claim 106 further including an epitaxial layer on the second major side of the n+ substrate.

108. An nn+ silicon epitaxial wafer as claimed in claim 107 wherein epitaxial layer is between 1 and 50 microns thick.

109. An nn+ silicon epitaxial wafer as claimed in any one of claims 106 to 108 wherein the thickness of the low stress LTO layer and the high stress LTO layer is between 1000 A and 10000 A.

110. An nn+ silicon epitaxial wafer as claimed in any one of claims 106 to 109 further including a polysilicon layer between the substrate and the low stress LTO layer.

111. An nn+ silicon epitaxial wafer as claimed in claim 110 wherein the thickness of the polysilicon layer is between 0.5 and 2 microns.

112. An nn+ silicon epitaxial wafer as claimed in any one of claims 106 to 111 wherein the warp is less than 50 microns.

113. An nn+ silicon epitaxial wafer as claimed in claim 112 wherein the warp is less than 20 microns.

114. An nn+ silicon epitaxial wafer as claimed in any one of claims 106 to 113 wherein the bow is less than 30 microns.

115. An nn+ silicon epitaxial wafer as claimed in claim 114 wherein the bow is less than 15 microns.

116. An nn+ silicon epitaxial wafer as claimed in any one of claims 106 to 115 wherein the haze performances is less than 50 ppm.

117. An nn+ silicon epitaxial wafer as claimed in claim 116 wherein the haze performance is less than 15 ppm.

118. An nn+ silicon epitaxial wafer as claimed in any one of claims 106 to 117 wherein the LLS performance greater than 0.128 microns is less than 100 per wafer.

119. An nn+ silicon epitaxial wafer as claimed in claim 118 wherein the LLS performance greater than 0.128 microns is less than 30 per wafer.

120. An nn+ silicon epitaxial wafer as claimed in any one of claims 106 to 119 wherein the LLS performance greater than 0.155 microns is less than 50 per wafer.

121. An nn+ silicon epitaxial wafer as claimed in claim 120 wherein the LLS performance greater than 0.155 microns is less than 10 per wafer.

122. An nn+ silicon epitaxial wafer as claimed in any one of claims 106 to 121 wherein the LLS performance greater than 0.193 microns is less than 30 per wafer.

123. An nn+ silicon epitaxial wafer as claimed in claim 122 wherein the LLS performance greater than 0.193 microns is less than 10 per wafer.

124. An nn+ silicon epitaxial wafer as claimed in any one of claims 106 to 123 wherein the LLS performance greater than 0.285 microns is less than 20 per wafer.

125. An nn+ silicon epitaxial wafer as claimed in claim 124 wherein the LLS performance greater than 0.285 microns is less than 5 per wafer.

126. An nn+ silicon epitaxial wafer as claimed in any one of claims 106 to 125 wherein the etch rate in wet bench cleaning is less than 100nm.

ABSTRACT

A two layer LTO backside seal for a wafer. The two layer LTO backside seal includes a low stress LTO layer having a first major side and a second major side, the first major side of the low stress LTO layer adjacent to one major side of the wafer. The two layer LTO backside seal further includes a high stress LTO layer having a first major side and second major side, the first major side of the high stress LTO layer adjacent the second major side of the low stress LTO layer.

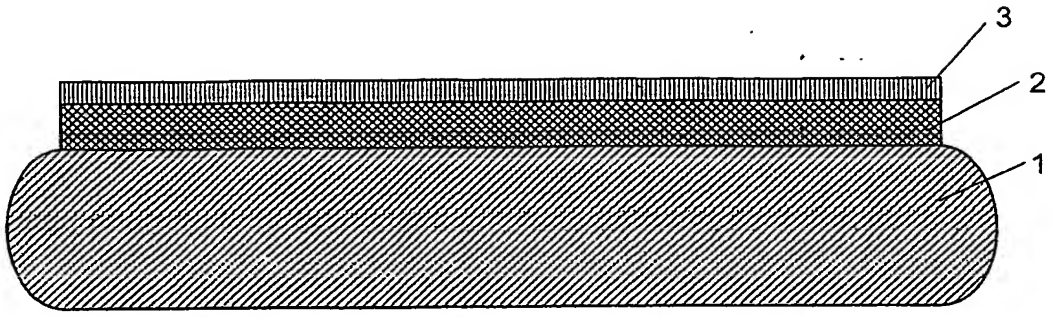

FIGURE 1

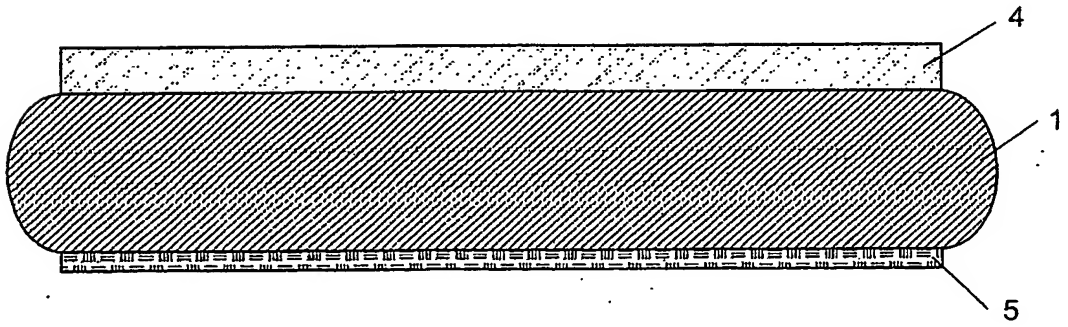

FIGURE 2